Analysis on the Performance Enhancement of Integrated Passives

Chan-Sei Yoo
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I. Overview on SoP
II. Integrated Passives : Inductor
III. Integrated Passives : Band Pass Filter
IV. Si-BCB Technology
V. Conclusion
System on Package

Active Integration Technology

- SOC
- SIP

Passive Integration Technology

- LTCC
- Hybrid Insertion
- MEMS

SOP

Source: Georgia Tech
Integrated Passives

New applications up to W-band (\(\sim110\)GHz)
Need high resolution for mm-wave \(\rightarrow\) SOP-D technology
Require low parasitic interconnection \(\rightarrow\) Flip-Chip Interconnection
Replace discrete components to High-Q embedded passives
Add functionality in the package \(\rightarrow\) Embedded Antenna
Layout examples of integrated inductor

- Transmission line
- Meander
- Loop
- Multi-layered
- Spiral
- Solenoid
Equivalent Circuit
Equivalent Circuit

Low-resistivity substrate

![Equivalent Circuit Diagram for Low-Resistivity Substrate]

High-resistivity substrate

![Equivalent Circuit Diagram for High-Resistivity Substrate]
\[ Q_L = Q_{\text{cond}} \cdot Q_{\text{sub}} \cdot Q_{\text{res}} \]

\[ Q_L = \frac{\omega L_S}{R_S} \cdot \frac{R_{LP}}{R_{LP} + \left( \frac{\omega L_S}{R_S} \right)^2 + 1} \cdot \frac{1}{R_S} \cdot \frac{R_S^2 (C_{fb} + C_{LP})}{L_S} - \omega^2 L_S (C_{fb} + C_{LP}) \]
\[ Q_L = Q_{\text{cond}} \times Q_{\text{sub}} \times Q_{\text{res}} \]
Q factor for high-resistivity substrate

\[ Q_L = \frac{\omega L_S}{R_S} \left[ 1 - \frac{R_S^2(C_{fb} + C_{LP})}{L_S} - \omega^2 L_S(C_{fb} + C_{LP}) \right] \]

- \( Q_{cond} \)
- \( Q_{res} \)

\[ f_{Q_{\text{max}}} = \frac{1}{2\pi} \sqrt{\frac{1}{3} \left[ \frac{1}{L_S(C_{fb} + C_{LP})} - \frac{R_S^2}{L_S^2} \right]} \]
\[ f_{Q = 0} = \frac{1}{2\pi} \sqrt{\left[ \frac{1}{L_S(C_{fb} + C_{LP})} - \frac{R_S^2}{L_S^2} \right]} \]

\[ f_{Q_{\text{max}}} = \sqrt{\frac{1}{3}} f_{Q = 0} \]
Q factor

Graphical interpretation

- $Q_L$ vs. $R_s$
- $Q_L$ vs. $C_G$
- $Q_L$ vs. $R_G$

Graphs showing $Q_L$ vs. frequency for different values of $R_s$, $C_G$, and $R_G$.
**Improving $Q_L$**

**Shape of Spiral Inductor**

**Circular vs. Rectangular**

<table>
<thead>
<tr>
<th>Actual shape</th>
<th>Circular</th>
<th>Rectangular</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image1.png" alt="Circular Inductor" /></td>
<td><img src="image2.png" alt="Rectangular Inductor" /></td>
<td></td>
</tr>
</tbody>
</table>

**Measured Performance**

<table>
<thead>
<tr>
<th>Type</th>
<th>$L_s$ (nH)</th>
<th>$f_{res}$ (GHz)</th>
<th>$Q_L$ @ 5GHz</th>
<th>$Q_{max}$</th>
<th>$f_{Q_{max}}$ (GHz)</th>
<th>$FOM$ (nH/mm$^2$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Circular</td>
<td>8.0</td>
<td>7.8</td>
<td>40</td>
<td>40</td>
<td>5</td>
<td>1097</td>
</tr>
<tr>
<td>Rectangular</td>
<td>6.8</td>
<td>8.5</td>
<td>34</td>
<td>34</td>
<td>5</td>
<td>792</td>
</tr>
</tbody>
</table>

(Ref: E Beyne, et al., “Spiral Inductors in Multi-layer Thin Film MCM-D,”
In IMAPS Europe, Krakow, Poland, pp.255-260. September 4-6, 2002.)
Improving $Q_L$

- Si technologies in which thin Al layers are replaced by Cu layers
- LTCC has an advantage over HTCC as high-conductivity metals such as Ag and Au
- MCM-D, in which thick Cu layers are preferred for the integration

![Graph showing $Q_L$ vs. Frequency (GHz) for different thicknesses (t) of the metal layers: t=5um, t=10um, t=15um, t=20um.](image)
Improving $Q_L$

By reducing the Substrate Losses

- Replacing the lossy silicon with a higher-quality dielectric like BCB
- Use of metal or resistive ground shields underneath the spiral inductor

Adding BCB layer 5um, 16um on 20$\Omega$-cm Si substrate
Improving $Q_L$

By lowering the Parasitic Capacitance to ground

- Low dielectric constant reduces the parasitic capacitance
  → increase in $Q_L$ factor
Influence of Layout Parameter

- **N**: # of turns, **R_{in}**: inner radius of the spiral

  ![Graph showing Q_{loss} vs. Frequency for N=2.5 and N=3.5](image)

  - **Q_{loss}** for same Ls (R_{in} deviation)

- **W**: width, **S**: spacing in between the coil

  Widening **W** → **Q_{L}** ↑

  Inner turns narrower → loss due to eddy current ↓ → **Q_{L}** ↑

- **D**: distance between spiral and ground

  ![Graph showing Ls vs. R_{in}](image)

  ![Graph showing C_{G} vs. Substrate thickness](image)

  ![Graph showing C_{G} vs. D_{inter}](image)

  **u-stripline** vs. **CPW**
## Integrated Inductor Examples

### Measured Performance

<table>
<thead>
<tr>
<th>N</th>
<th>W(um)</th>
<th>S(um)</th>
<th>Rin(um)</th>
<th>Dout(um)</th>
<th>Ls(nH)</th>
<th>Qmax</th>
<th>FQmax(GHz)</th>
<th>Fres(GHz)</th>
<th>Area(mm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.5</td>
<td>30</td>
<td>20</td>
<td>100</td>
<td>200</td>
<td>0.65</td>
<td>&gt;200</td>
<td>18.9</td>
<td>46.3</td>
<td>0.395</td>
</tr>
<tr>
<td>1.5</td>
<td>30</td>
<td>20</td>
<td>100</td>
<td>200</td>
<td>1.55</td>
<td>110</td>
<td>13.0</td>
<td>22.5</td>
<td>0.515</td>
</tr>
<tr>
<td>2.5</td>
<td>30</td>
<td>20</td>
<td>100</td>
<td>200</td>
<td>3.36</td>
<td>61</td>
<td>6.3</td>
<td>13.0</td>
<td>0.650</td>
</tr>
<tr>
<td>3.5</td>
<td>30</td>
<td>20</td>
<td>100</td>
<td>200</td>
<td>6.15</td>
<td>48</td>
<td>4.4</td>
<td>7.8</td>
<td>0.801</td>
</tr>
<tr>
<td>4.5</td>
<td>30</td>
<td>20</td>
<td>100</td>
<td>200</td>
<td>10.08</td>
<td>40</td>
<td>2.8</td>
<td>5.3</td>
<td>0.967</td>
</tr>
<tr>
<td>5.5</td>
<td>30</td>
<td>20</td>
<td>100</td>
<td>200</td>
<td>14.77</td>
<td>37</td>
<td>2.0</td>
<td>4.0</td>
<td>1.149</td>
</tr>
</tbody>
</table>

- Ni/Au component layer
- 2 μm Ti/Cu metal-3
- 3 μm Ti/Cu/Ti metal-2
- 1 μm top Al contact metal-1
- 1 μm bottom Al contact metal-1
- TaN- resistor
- 5 μm BCB-2
- 5 μm BCB-1
- Ta₂O₅ capacitor
- 700 μm Glass substrate
### Integrated Inductor Examples

**LTCC**

#### Measured Performance

<table>
<thead>
<tr>
<th>N</th>
<th>W(um)</th>
<th>Height from ground(um)</th>
<th>Ls(nH)</th>
<th>Qmax</th>
<th>FQmax(GHz)</th>
<th>Fres(GHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>100</td>
<td>180</td>
<td>4.8</td>
<td>37</td>
<td>1.3</td>
<td>2.9</td>
</tr>
<tr>
<td>2</td>
<td>100</td>
<td>360</td>
<td>6.1</td>
<td>47</td>
<td>1.3</td>
<td>3.2</td>
</tr>
<tr>
<td>2</td>
<td>100</td>
<td>540</td>
<td>6.7</td>
<td>52</td>
<td>1.3</td>
<td>3.25</td>
</tr>
</tbody>
</table>

- **Dupont 951AT**: \( E_r = 7.8 \)
- \( W_{minimum} = 100\mu m \)
Use of Inductors in Circuits

2nd order BPF

Circuit

Actual Shape

S-parameter Magnitude

return loss

insertion loss

0 dB

Q = 127

Q = 35

Q = 24

-30 dB

1 GHz

10 GHz

Frequency
Band Pass Filter in Si-BCB technology(I)

Ti : for the adhesion between Au and dielectric

**Band Pass Filter in Si-BCB technology(1)**

**Filter Design**

- **Specification**

4\textsuperscript{th}-order BPF topology: ideal TRL

4\textsuperscript{th}-order BPF topology: actual TRL


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**Millimeterwave Devices & Circuits Lab**
Filter Response

BCB thickness variation: simulated

Measured vs. Simulated

Band Pass Filter in Si-BCB technology (II)

**Structure**

- **W=0.43mm**
  - Er=2.65
  - Er=2.65
  - Er=11.9
  - 10um 4um 10um 400um

- **W=10um**
  - Er=2.65
  - Er=2.65
  - Er=11.9
  - 10um 4um 10um 400um

**Filter Design**

- Capacitive section
  - Zc=5 Ω
  - Er,eff=2.55

- Inductive section
  - Z_L=208 Ω
  - Er,eff=2.95

- Resonator and inverters are replaced by C-L-C semi-lumped lowpass filter
- Control the attenuation band
- Size can be minimized
  (C-L-C semi-lumped LPF is smaller than quarter wavelength inverter)

Band Pass Filter in Si-BCB technology

Filter Response

- Circuit Simulation
- Measurement vs. Structure Simulation
- Actual Shape

Ref: C. Quendo, et al., “Miniaturized and Out-of-Band Improved Bandpass Filter in Si-BCB Technology,”
IEEE MTT-S Digest, p1475-1478, 2004
Si- BCB technology in IMEC

Si- BCB technology in IMEC

Features

- W=77um, S=20um
- I.L. = 0.2 dB/mm @ 60GHz

Measured

Cross-section of CPW

Ref: W. De Raedt, et al., “Multi-layer Thin-Film MCM-D for the Realization of Q- and V-band Functions,”
IEEE MTT-S Digest, p1151-1154, 2003
Si-BCB technology in IMEC

Wilkinson Power Divider

- $f_0 : 40$ GHz (Q band)
- Size: $0.6 \times 1.2$ mm$^2$

Si-BCB technology in IMEC

Quadrature Coupler

- fo: 60 GHz (Q band)
- Edge Coupled line:
  - W=40um, S=5um

Actual Shape

Return Loss

Insertion Loss & Isolation

Ref: W. De Raedt, et al., “Multi-layer Thin-Film MCM-D for the Realization of Q- and V-band Functions,”
IEEE MTT-S Digest, p1151-1154, 2003
Si- BCB technology in IMEC

- fo : 30 GHz (Ka band)
- 3 Coupled CPW line + 4 Interdigital capacitors

Ref: W. De Raedt, et al., “Multi-layer Thin-Film MCM-D for the Realization of Q- and V-band Functions,”
IEEE MTT-S Digest, p1151-1154, 2003
Conclusions

I. SoP- D is adequate method for mm-Wave packaging.

II. Inductor can be optimized by adjusting lay-out parameter; width, space, $R_{in}$, $D_{out}(CPW)$

III. BPF can be evaluated by Si-BCB technology and its response is quite good for mm-Wave application.

IV. Other passives like coupler, divider can be integrated by SoP- D multilayer technology