Novel Sloped Etch Process for 15nm InAlAs/InGaAs Metamorphic HEMTs

Seong-Jin Yeon1, Myunghwan Park, and Kwang-Seok Seo

Seoul National Univ., School Of Electrical Engineering and Computer Science
San 56-1, Shillim-dong, Kwanak-ku, Seoul 151-744, Korea

Phone: +82-2-877-0298 E-mail: realzeratol@hanmail.net

Abstract - We developed a new technology that reduces gate length with modified sloped etch process to fabricate nanometer scale high-electron mobility transistors (HEMTs). The polymer deposition and Si$_3$N$_4$ etching with positive slope make this technology realizable. A HEMT with this technology has merits of both fine length definition beyond the limit of an electron beam (E-beam) lithography system and overcoming the metal filling problem caused by a high aspect ratio. Using this technology, we could get 15nm gate length from initial 40nm line pattern. The fabricated 15nm InAlAs/InGaAs metamorphic HEMTs (MHEMTs) have high DC and RF performance characteristics, a transconductance of 1.6 S/mm, a cutoff frequency $f_T$ of 580 GHz.

Keywords — modified sloped etch process, High-electron mobility transistors, E-beam lithography, Metamorphic HEMTs, cutoff frequency, transconductance

I. INTRODUCTION

InAlAs/InGaAs high-electron mobility transistors are the most promising devices that can operate in the high RF range, owing to their high electron mobilities, saturation velocities, and sheet electron densities [1]. Many groups reported superior RF characteristics of InP-based HEMTs by reducing gate length [2]-[3]. Recently, there have been similar works on going using metamorphic HEMT structure on GaAs substrate for the benefit of economic cost. However, it is indispensable to use high resolution E-beam lithography system in order to reduce gate length. In addition, the gate metal filling has been issued for gate pattern smaller than 50 nm due to the high aspect ratio. Hence, various technologies such as sloped etch process, side wall process, and E-beam resist flowing process have been developed to solve this problem [4].

In this work, we propose a new technology that reduces gate length and widens the opening of gate stem through several etch processes. From this process, initial gate length of 40 nm was reduced to 15 nm and gate metal could be well deposited for gate pattern smaller than 50 nm. This process enables us to achieve narrow gate length beyond the limit of E-beam lithography and metal evaporation.

II. DEVICE FABRICATION

In$_{0.75}$GaAs/In$_{0.52}$AlAs metamorphic HEMT layers were grown by molecular beam epitaxy (MBE) on a GaAs substrate - a mobility of 10,100 cm$^2$/V-s and a sheet carrier density of 3.56x10$^{12}$ cm$^{-2}$ at 300 K. The epitaxial structure is shown in Fig. 1. To lower sheet resistance, delta doping layers of 2x10$^{13}$ cm$^{-2}$ were applied in every 25 Å spacing inside upper InGaAs and InP cap layer. Indium molefraction of 75 % is applied to channel material and barrier thickness is lowered to 30 Å to improve RF performance.

Fig. 1. Metamorphic HEMT epitaxial structure. To lower sheet resistance, delta doping layers of 2x10$^{13}$ cm$^{-2}$ were applied in every 25 Å spacing inside upper InGaAs and InP cap layer.

The fabrication process is as follows. The process begins with mesa isolation using phosphoric etchant. For ohmic electrodes, Ni/Ge/Au were evaporated and followed by rapid thermal annealing at 320 °C for 30 s. The ohmic contact resistance and sheet resistance were 0.015 $\Omega\cdot$cm$^2$ and 45 $\Omega\cdot$cm$^{-1}$, respectively. We modified gate process sequences from conventional HEMTs process because of metal spreading in gate foot area and exposure in recessed area. The conventional gate process is as follows. The gate patterning is followed by recess sequence and gate metal evaporation at the end. When gate metal is evaporated, recessed void gives space that could be spread to metal vapor, thus final gate length ($L_g$) is extended. Also after HEMTs fabrication, recessed area near gate may degrade device characteristics and reliability characteristics, which are critical for the nano HEMTs performances. To solve this problem, gate recess process is finished before gate dielectric deposition. Through these sequences, recessed surface is protected by Si$_3$N$_4$ layer and final gate length is not extended due to the removal of recessed void. The modified gate structure is shown in fig. 2. The gate recess in the InGaAs cap layer was performed by the citric acid solution with an ultrasonic assist of 5 sec and consecutively without an ultrasonic assist for the rest of the time. The recess with ultrasonic assist was conducted under conditions of 35 KHZ and 3.5 W in ultrasonic bath [5]. The InP cap layer was recessed by HCl solution (HCl: phosphoric acid: H$_2$O=1:1:1). Using remote plasma enhanced chemical
vapor deposition (RPECVD), we deposited a Si$_3$N$_4$ (300 Å) film as a passivation layer and also as a medium for gate length reduction. The initial gate pattern of 40 nm length was defined by electron beam lithography (100 keV JBX-9300) using ZEP/PMGI/ZEP tri-layer and double exposure/double develop method.

III. GATE DIELECTRIC ETCHING PROCESS

In terms of gate dielectric etching, SF$_6$/Ar plasma induces a positive slope of Si$_3$N$_4$ which results in gate length reduction, but on the other hand, etches the interface between EB resist and dielectric layer (Fig. 3). Therefore, we cannot use this merit of reducing gate length. To make the good use of former advantage, we have developed various gate dielectric etching process. Fig. 4, is a scheme of sloped etch process, which is slightly modified compared to previous reported process [6] for initial narrow pattern more than 50 nm. The process sequences are like this.

We developed modified sloped etch process based on SF$_6$/Ar plasma (Fig. 5) which results in less plasma damage. The process sequences are as follows. First, polymer is conformally deposited on T-gate pattern using CH$_4$/H$_2$ plasma (Fig. 5(a)). This polymer not only reduces length of gate stem but also protects interface between EB resist and dielectric layer from etching in SF$_6$/Ar plasma. Secondly, a vertical etching removes polymer in the center of gate foot (Fig. 5(b)). The polymer at the side wall of gate stem is less etched than the center of gate foot because CF$_4$/H$_2$ plasma etches polymer in a vertical direction at low pressure. Consequently, the polymer is remained in the corners around the interface between EB resist and dielectric layer. Finally, SF$_6$ based plasma etches bottom Si$_3$N$_4$ layer with a positive slope which results in gate length reduction stably because the residual polymer in the corners prevents from etching the interface. In addition, the opening of gate stem is widened because the uncovered part of gate stem is etched in SF$_6$/Ar plasma (Fig. 2c).

Through this new process, gate length is reduced from 40 nm to 15 nm, and widened opening of gate stem makes metal filling easy (Fig. 6).
After gate foot formation, bottom InGaAs cap layer (20 Å), for reducing surface effect, is wet-etched by phosphoric acid. And then, InP etch stopper on the barrier was etched in Ar gas to reduce the gate to channel distance. Finally, the Ti/Pt/Au gate metal was evaporated and lifted off.

IV. DEVICE CHARACTERISTICS.

The 15 nm MHEMTs were measured at RT to determine their DC and RF characteristics. Transconductance characteristics are shown in Fig. 7. The plot represents that an increase of Gm and negative shift of Vth are due to the reduction of plasma damage when final etching is changed from CF4/O2 to SF6/Ar plasma. Also, in the fig. 8, the reduction of damage is shown by decrease of ideality factor when final etching is performed by SF6/Ar plasma. The fabricated 15nm MHEMTs using previous sloped etch process have relatively low DC and RF performance characteristics compared to modified sloped etch process, a transconductance of 1.43 S/mm, a cutoff frequency fT of 490 GHz. This can be due to plasma damage induced by CF4/O2 plasma. The reasons why effect of the plasma damage is more significantly occurred compared to previous reported characteristics [6] can be understood as follows. Plasma etching through narrow pattern with relatively high aspect ratio needs sufficient over-etching for pattern to be transferred clearly. Therefore, the increased etching time might have caused damage on the devices. And as gate length is reduced, damage effect is more dominant on device characteristics, thus degrading device performance. The DC and RF characteristics of 15 nm MHEMTs using modified sloped etch process were plotted in fig. 9 and fig. 10, respectively. The pinch-off voltage was -0.4 V. The maximum saturated current was about 800 mA/mm and the maximum transconductance Gm,max was about 1.6 S/mm. The RF characteristics were determined by RT on-wafer measurement at frequencies up to 50 GHz using an HP8510C vector network analyzer and on-wafer probes. Fig. 5 shows the frequency dependence of the current gain H21, and the MAG/MSG of the 15 nm gate MHEMT at Vd=0.8 V and Vgs=0 V. We obtained the unit current gain frequency fT of 580 GHz by extrapolating H21 with a slope of -20 dB/decade. The maximum oscillation frequency fmax was estimated to be about 320 GHz from MAG/MSG.

V. CONCLUSION

We developed modified sloped etch process with less plasma damage. By this technology, we obtained a 15 nm gate length from the initial 40 nm gate pattern. In addition, a line length reduction of more than 60% enabled us to overcome the limit of E-beam lithography system. The fabricated devices have high DC and RF performances characteristics, a transconductance of 1.6 S/mm, a maximum saturated current of 800 mA/mm, a maximum oscillation frequency fmax of 320GHz, and a cutoff frequency fT of 580 GHz.

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**Fig. 9.** Current-voltage (I-V) characteristics of a 15 nm-gate metamorphic HEMT with modified sloped etch process. The gate-source voltage $V_{gs}$ was decreased from 0.3 (top) to -0.4 V (bottom) in -0.1 V steps.

**Fig. 10.** Frequency characteristics of the current gain $|h_{21}|^2$, MAG/MSG for a 15-nm-gate metamorphic HEMT with modified sloped etch process. The drain-source voltage $V_{ds}$ was 0.8 V, and the gate-source voltage $V_{gs}$ was 0 V. A $f_T$ of 580 GHz was obtained by extrapolating $|h_{21}|^2$ with a slope of -20dB/decade. A $f_{max}$ was estimated to be about 320 GHz from the MAS/MSG.